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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,943	06/26/2003	Victor J. Stolpman	873.0124.U1(US)	7557

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HARRINGTON & SMITH, LLP
4 RESEARCH DRIVE
SHELTON, CT 06484-6212

EXAMINER

BAKER, STEPHEN M

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/608,943

Applicant(s)

STOLPMAN, VICTOR J.

Examiner

Stephen M. Baker

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 14-19 is/are allowed.
- 6) ☒ Claim(s) 1-13 and 20-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

In the description of prior art FIG. 2A, "LDPC mothercode 37A" (two occurrences) apparently should be "LDPC mother code definition 37A" or the like, as "mothercode" is customarily the un-punctured coded output of the LDPC encoder; in the summary of the invention, "storing an error reduction code mother code" apparently should be "storing an error reduction code mother code definition" or the like, "this is an LDPC mother code such as a parity check matrix" apparently should be "this is an LDPC mother code definition such as a parity check matrix" or the like, and "storing a LDPC mother code" apparently should be "storing a LDPC mother code definition" or the like; in the description of FIG. 2B, "LDPC mother code 37B" (two occurrences) apparently should be "LDPC mother code definition 37B" or the like.

The disclosure apparently makes it needlessly difficult to perceive that the "puncturing sequences" described may be no different than stored bits of puncturing masks wherein the positions of stored "1" values designate positions of bits to be punctured and the positions of stored "1" values designate positions of bits to be punctured. The utility and enablement of storing and applying "degrees," at least as the term "degree" is applied in FIG. 1B, for identifying puncturing locations is not clearly explained, and is not understood unless a "degree" is interpreted as a codeword polynomial coefficient degree. Where applicant refers to "subsets" of a puncturing

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sequence, it is assumed that subsets of puncturing locations (subsets of "1" values in the puncturing sequence, with the remaining "1" values treated as "0" values) are being referred to. Where applicant states that "(t)he puncturing sequence S_{\max} may or may not be the entire matrix H" applicant apparently means that the puncturing sequence S_{\max} may or may not have a length of N, the number of columns in the H matrix. As the number of puncturing sequences (N-K) matches the number of bits by which the LDPC code (N bits) is longer than the uncoded data (K bits), it is presumed that the LDPC code is systematic (i.e. the LDPC encoder adds N-K parity bits to the original data to form the LDPC code) and that the only bits punctured are parity bits.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-13 and 20-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 11, 12, 20 and 23: "a memory for storing a mother code" is apparently elliptical, as the "mother code" is understood to be the un-punctured coded output of the LDPC encoder, and so apparently should read as "a memory for storing a mother code definition" or the like.

Regarding claim 4: "two subsets S_i that is a puncture sequence for a code rate R_i " apparently should be "two subsets S_i that are puncture sequences for code rates R_i ".

Allowable Subject Matter

4. The indicated allowability of claims 7-10 is withdrawn in view of the newly discovered reference to Mantha *et al.* Rejections based on the newly cited reference follow.
5. Claims 11-13 would be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.
6. Claims 14-19 are allowed.

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
8. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over the published article to Cox *et al* (hereafter "Cox").

Cox discloses an encoder for generating framed (terminated) rate-compatibly punctured convolutional codes (which are "error reduction codes"), implemented by a programmable DSP. Each terminated punctured codeword so generated is "a codeword defining N codeword elements and K information elements coded at a code rate $R=K/(N-P)$, wherein P is a number of punctured elements of the codeword". The processes of generating the mother code and of puncturing the mother code are

shown by Cox as being performed in two separate stages (figure 7). The puncturing process shown by Cox uses a puncturing table. Because the codes are punctured rate-compatibly, the puncturing patterns used by Cox must be such that " S_{\max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1 " (sic).

Regarding claim 1, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the rate-compatible punctured convolutional coding disclosed by Cox by using a "first storage location for storing an error reduction code mother code" and a "second storage location for storing a maximum puncturing sequence S_{\max} " because the processes of generating the mother code and of puncturing the mother code are shown by Cox as being performed separately, and furthermore because the rate-compatible punctured convolutional coding disclosed by Cox is implemented by a processor with programmed instructions requiring storage locations. A region of DSP program memory with instructions for implementing the mother code encoding process shown by Cox would provide "a first storage location for storing an error reduction code mother code" and a region of DSP memory for storing the puncturing process table shown by Cox for the highest rate rate-compatible puncturing scheme would provide "a second storage location for storing a maximum puncturing sequence S_{\max} ".

Regarding claim 2, the DSP for implementing the rate-compatible punctured convolutional coding disclosed by Cox implements processing for both transmitting and receiving the punctured convolutional codes.

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9. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the published article to Kim *et al* (hereafter "Kim").

Kim discloses an encoder for generating framed (terminated) rate-compatibly punctured convolutional codes (which are "error reduction codes"). Each terminated punctured codeword so generated is "a codeword defining N codeword elements and K information elements coded at a code rate $R-K/(N-P)$, wherein P is a number of punctured elements of the codeword". The processes of generating the mother code (figure 1) and of subsequently puncturing the mother code (figure 2) are described by Kim as being performed in two separate stages. The puncturing process shown by Kim uses a puncturing table. Because the codes are punctured rate-compatibly, the puncturing patterns used by Kim must be such that " S_{\max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1 " (sic).

Regarding claim 1, Official Notice is given that the convenience of implementing a channel coder by means of a processor with programmed instructions was well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the rate-compatible punctured convolutional coding disclosed by Kim by using a "first storage location for storing an error reduction code mother code" and a "second storage location for storing a maximum puncturing sequence S_{\max} " because the process of generating the mother code and of puncturing the mother code are shown by Kim as being performed separately, and because the convenience of implementing a channel coder by means of a processor with programmed instructions was already

well known. A region of program memory with instructions for implementing the mother code encoding process shown by Kim would provide "a first storage location for storing an error reduction code mother code" and a region of processor memory for storing the puncturing process table shown by Kim for the highest rate rate-compatible puncturing scheme would provide "a second storage location for storing a maximum puncturing sequence S_{max} ".

Regarding claim 2, the rate-compatible punctured convolutional coding disclosed by Kim is part of a transmitter for transmitting the punctured convolutional codes.

Regarding claim 3, Kim shows (figure 2) a punctured code with all parity bits punctured (PT_0).

Regarding claims 4-6, Kim shows (figure 2) five different code rates, with the codes collectively meeting the recited puncturing limitations.

10. Claims 1, 2, 4-10 and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0126551 to Mantha *et al* (hereafter "Mantha").

Mantha discloses an encoder for generating rate-compatibly punctured LDPCs, implemented by software. Each punctured LDPC codeword so generated is "a codeword defining N codeword elements and K information elements coded at a code rate $R=K/(N-P)$, wherein P is a number of punctured elements of the codeword". The processes of generating the mother code (figure 1) and of subsequently puncturing the mother code (figure 2) are described by Mantha as being performed in two

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separate stages. Mantha describes the use of a puncturing table as "typical" [0136] and instead uses an algorithm based on two parameters in order to generate the puncturing patterns. Because the codes are punctured rate-compatibly, the puncturing patterns used by Mantha must be such that " S_{\max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1 " (sic) [0127].

Regarding claim 1, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the rate-compatible punctured LDPC encoding disclosed by Mantha by using a "first storage location for storing an error reduction code mother code" and a "second storage location for storing a maximum puncturing sequence S_{\max} " because the process of generating the mother code and of puncturing the mother code are shown by Kim as being performed separately, because Kim teaches the use of puncturing tables storing puncturing sequences to be "typical," and because the encoder is implemented by software. A region of program memory with instructions for implementing the mother code encoding process shown by Mantha would provide "a first storage location for storing an error reduction code mother code" and a region of processor memory for storing the puncturing process table shown by Mantha for the highest rate rate-compatible puncturing scheme would provide "a second storage location for storing a maximum puncturing sequence S_{\max} ".

Regarding claim 2, the rate-compatible punctured convolutional coding disclosed by Mantha is part of a transmitter for transmitting the punctured convolutional codes.

Regarding claims 4-6, Mantha shows [0142] six different code rates, with the codes collectively meeting the recited puncturing limitations.

Regarding claims 7 and 9, each bit of the LDPC code is a “variable” having a codeword polynomial coefficient “degree”, and so a bit of a stored puncturing pattern corresponding to bit position in the codeword would be stored in a “memory element storing a variable degree”.

Regarding claims 8 and 9, each systematic (i.e. non-parity) bit of the LDPC code corresponds to a “variable node”.

Response to Arguments

11. Applicant's arguments filed 10 June 2005 have been fully considered but they are not persuasive.

Applicant argues that a “teaching that the *puncture table* is used to achieve a maximum code rate and a subset of *it* is used to achieve a minimum code rate” (italics added) is required to reject the claims, as if the argued “subset of it” is a subset of the “puncture table”, whereas the relevant portion of the claims, in contrast, appear to merely refer to a subset of the puncturing pattern rather than a subset of the puncturing table and thereby provide a limitation that would apply to the set of puncturing patterns for any rate-compatible puncturing scheme.

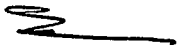
Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Stephen M. Baker
Primary Examiner
Art Unit 2133

smb